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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/973,795	10/11/2001	Kazuya Ono	A319-1	7244

466 7590 04/21/2005

YOUNG & THOMPSON
745 SOUTH 23RD STREET
2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/973,795	ONO, KAZUYA	
	Examiner	Art Unit	
	Michael C. Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *2,7,11 and 16* is/are withdrawn from consideration.

5)☒ Claim(s) *6,8,9,21 and 25* is/are allowed.

6)☒ Claim(s) *1,3-5,10,12-15,17-20,22-24 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Office Action

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 3 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 3 recites the limitation "the *n* bit wide parallel data segments" in lines 5-6. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination, the Examiner will interpret this limitation as "*n* bit wide parallel data segments".

4. Claim 12 recites the limitation "the *n* bit wide parallel data segments" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination, the Examiner will interpret this limitation as "*n* bit wide parallel data segments".

Claim Objections

5. Claim 6 is objected to because of the following informalities: in claim 6, line 10, "a generated an error correcting code" should be changed to "a generated error correcting code". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 3, 4, 12, 13, 20, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Rub, U.S. Patent 6,804,805 B2.

Referring to claim 3:

a. In column 6, lines 15-19, Rub discloses that the parallel-to-serial converter receives the successive ECC code words, converts each ECC code word into a serial representation and concatenates the serial representations to produce a serial stream of ECC code word bits (serial data with an error correcting code transmitted through a serial bus). Further, in column 6, lines 41-44, Rub discloses that the serial-parallel converter groups the bits into ECC code words and converts the ECC code words from a serial format to a parallel format (a serial-parallel converter which converts serial data with an error correcting code transmitted through said serial bus into parallel arrangement of *n* bit wide parallel data segments and the error correcting code).

b. In column 6, lines 46-55, Rub discloses that the ECC code words are sent to an ECC decoder and correction circuit to determine whether any of the ECC

symbols contains an error (an error detector which checks the error correcting code within said parallel data).

c. In column 6, lines 59-64, Rub discloses that the data field is then stripped from the recovered ECC code word to recover the original block of data code words, which is then provided to decoder. Bit-level decoder uses the inverse of the coding rules used by encoder to decode the successive data code words into respective data words (a parallel bus interface circuit that demultiplexes the *n* bit wide parallel data segments from the error detector into *m* bit wide parallel data on the parallel bus).

Referring to claim 4, in column 6, lines 55-58, Rub discloses that as long as the number of symbols containing an error is not greater than the maximum number of symbols that can be corrected, the original ECC symbols are recovered (wherein said error detector has a function of correcting said error when said error is detected by said error detector).

Referring to claim 12:

a. In column 6, lines 15-19, Rub discloses that the parallel-to-serial converter receives the successive ECC code words, converts each ECC code word into a serial representation and concatenates the serial representations to produce a serial stream of ECC code word bits (serial data with an included error correcting code). Further, in column 6, lines 41-44, Rub discloses that the serial-parallel converter groups the bits into ECC code words and converts the ECC code words from a serial format to a parallel format (converting serial data with an

included error correcting code into parallel arrangement of *n* bit wide parallel data segments and the error correcting code).

b. In column 6, lines 46-55, Rub discloses that the ECC code words are sent to an ECC decoder and correction circuit to determine whether any of the ECC symbols contains an error (checking the error correcting code applied to each said parallel data segment checking for an error based on said error correcting code).

c. In column 6, lines 59-64, Rub discloses that the data field is then stripped from the recovered ECC code word to recover the original block of data code words, which is then provided to decoder. Bit-level decoder uses the inverse of the coding rules used by encoder to decode the successive data code words into respective data words (demultiplexing the *n* bit wide parallel data segments into *m* bit wide parallel data on the parallel bus, wherein $m > n$).

Referring to claim 13, in column 6, lines 55-58, Rub discloses that as long as the number of symbols containing an error is not greater than the maximum number of symbols that can be corrected, the original ECC symbols are recovered (the step of correcting said error detected in said error checking step).

Referring to claims 20 and 23, in column 5, lines 4-5, Rub discloses that each data word can include any number of bits ($m = 32$ and $n = 8$).

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims 1, 10, 19, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Götze et al., U.S. Patent 4,450,561, and further in view of Carlton et al., U.S. Patent 4,218,742.

Referring to claim 1:

a. In column 3, lines 17-21, Götze et al. disclose that the data to be encoded or checked are applied to a byte selection logic and in column 4, lines 63-64, Götze et al. disclose that the byte selection logic consists of a series of multiplexers (a parallel bus interface circuit that receives as an input *m* bit wide data from the parallel bus and multiplexes the *m* bit wide data into sequentially generated *n* bit wide parallel data segments, with $n < m$).

b. In column 1, lines 49-52, Götze et al. disclose that each of the check bits of an ECC codeword is generated in parallel in a byte serial sequence and in column 3, lines 19-20, Götze et al. disclose that the check bits are generated byte-wise (a check bit producer that receives as an input the *n* bit wide parallel data segments and produces as an output a parallel arrangement of the *n* bit wide parallel data segments and a generated error correcting code).

c. In Figure 4, Götze et al. disclose outputting the check bits in parallel, however, Götze et al. don't explicitly disclose a parallel-serial converter, which

converts, said parallel arrangement of the *n* bit wide parallel data segments and the error correcting code from said check bit producer into serial data. In column 1, lines 12-18, Carlton et al. disclose that various arrangements are known in the art fro transferring data which is received at a disk file controller in parallel by bit form to a disk file in serial by bit form to be written on one of the tracks. It would have been obvious to one of ordinary skill at the time of the invention to include the parallel-serial conversion of Carlton et al. into the system of Götze et al. A person of ordinary skill in the art would have been motivated to make the modification because it is important to include ECC bits when writing and reading data to insure data integrity. Therefore, ECC bits of Götze et al. would be needed in the system of Carlton et al. Further, the system of Carlton et al. provides a means of changing the parallel ECC bits into a serial stream that can be used by most disk drives.

Referring to claim 10:

a. In column 3, lines 17-21, Götze et al. disclose that the data to be encoded or checked are applied to a byte selection logic and in column 4, lines 63-64, Götze et al. disclose that the byte selection logic consists of a series of multiplexers (multiplexing *m* bit wide parallel data sequentially into *n* bit wide parallel data segments, where $m > n$).

b. In column 1, lines 49-52, Götze et al. disclose that each of the check bits of an ECC codeword is generated in parallel in a byte serial sequence and in column 3, lines 19-20, Götze et al. disclose that the check bits are generated

byte-wise (applying an error correcting code to each *n* bit wide parallel data segment).

c. In Figure 4, Götze et al. disclose outputting the check bits in parallel, however, Götze et al. don't explicitly disclose converting said parallel data with the error correcting code into serial data. In column 1, lines 12-18, Carlton et al. disclose that various arrangements are known in the art fro transferring data which is received at a disk file controller in parallel by bit form to a disk file in serial by bit form to be written on one of the tracks. It would have been obvious to one of ordinary skill at the time of the invention to include the parallel-serial conversion of Carlton et al. into the system of Götze et al. A person of ordinary skill in the art would have been motivated to make the modification because it is important to include ECC bits when writing and reading data to insure data integrity. Therefore, ECC bits of Götze et al. would be needed in the system of Carlton et al. Further, the system of Carlton et al. provides a means of changing the parallel ECC bits into a serial stream that can be used by most disk drives.

Referring to claims 19 and 22, in column 3, lines 24-25, Götze et al. disclose that the data word is to comprise eight data bytes having eight data bits each ($n = 8$) and in column 4, lines 15-18, Götze et al. disclose the width of the bus being 4 bytes ($m = 32$).

10. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rub, U.S. Patent 6,804,805 B2, and further in view of Götze et al., U.S. Patent 4,450,561.

Referring to claims 5 and 14, in column 6, lines 55-58, Rub discloses that as long as the number of symbols containing an error is not greater than the maximum number of symbols that can be corrected, the original ECC symbols are recovered. However, Rub doesn't explicitly disclose that said error detector corrects said error when said error is a 1-bit error, and abandons an access when said error is a 2-bit error. In column 3, lines 4-6, Götze et al. disclose that most ECC devices are structured in such a manner that single errors can be corrected (said error detector corrects said error when said error is a 1-bit error). Further, in column 6, lines 39-42, Götze et al. disclose that a double error can be detected but not corrected (said error detector abandons an access when said error is a 2-bit error). It would have been obvious to one of ordinary skill at the time of the invention to include the correction of 1-bit errors and the abandonment of 2-bit errors of Götze et al. into the system of Rub. A person of ordinary skill in the art would have been motivated to make the modification because it is well-known that most ECC devices are structured in such a manner that single errors can be corrected (see Götze et al.: column 3, lines 4-6) and it is common for double errors to be difficult to correct because of the inability to find the bits that are incorrect (see Götze et al.: column 6, lines 31-42 and Rub: column 6, lines 55-59).

11. Claims 15, 17, 18, 24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rub, U.S. Patent 6,804,805 B2, and further in view of Götze et al., U.S. Patent 4,450,561.

Referring to claim 15:

a. In column 6, lines 15-20, Rub discloses that the parallel-to-serial converter receives the successive ECC code words and converts each ECC code word into a serial representation and concatenates the serial representations to produce a serial stream of ECC code word bits. However, Rub doesn't explicitly disclose multiplexing *m* bit wide parallel data from the parallel bus into *n* bit wide segments, where $m > n$ and applying an error correcting code to each parallel data segment. In column 1, lines 49-52, Götze et al. disclose that each of the check bits of an ECC codeword is generated in parallel in a byte serial sequence. It would have been obvious to one of ordinary skill at the time of the invention to include the byte-wise check bit generator of Götze et al. into the system of Rub. A person of ordinary skill in the art would have been motivated to make the modification because it permits a structuring of the ECC device so that it has general application (see Götze et al.: column 1, lines 49-52).

b. In column 6, lines 42-49, Rub discloses that serial-to-parallel converter groups the bits into ECC code words and converts the ECC code words from a serial format to a parallel format. Serial-to-parallel converter then outputs the successively recovered ECC code words in parallel format to ECC decoder and correction circuit (converting serial data with included error codes transmitted through said serial bus into parallel arrangement of the *n* bit wide parallel data segments and the error correcting code.

c. In column 6, lines 46-55, Rub discloses that the ECC code words are sent to an ECC decoder and correction circuit to determine whether any of the ECC

symbols contains an error (checking the error correcting code applied to each parallel data segment).

d. In column 6, lines 59-64, Rub discloses that the data field is then stripped from the recovered ECC code word to recover the original block of data code words, which is then provided to decoder. Bit-level decoder uses the inverse of the coding rules used by encoder to decode the successive data code words into respective data words (demultiplexing the *n* bit wide parallel data segments into *m* bit wide parallel data on the parallel bus).

Referring to claim 17, in column 3, lines 4-6, Götze et al. disclose that most ECC devices are structured in such a manner that single errors can be corrected (said error detector has a function of correcting said error when said error is detected by said error detector).

Referring to claim 18, in column 3, lines 4-6, Götze et al. disclose that most ECC devices are structured in such a manner that single errors can be corrected (said error detector corrects said error when said error is a 1-bit error). Further, in column 6, lines 39-42, Götze et al. disclose that a double error can be detected but not corrected (said error detector abandons an access when said error is a 2-bit error).

Referring to claim 24, in column 3, lines 24-25, Götze et al. disclose that the data word is to comprise eight data bytes having eight data bits each ($n = 8$) and in column 4, lines 15-18, Götze et al. disclose the width of the bus being 4 bytes ($m = 32$).

Referring to claim 26, in Figure 2, Rub discloses that the *n* bit wide segments transferred while communicating from the parallel bus to the serial bus follow a different

path than that used to transfer the *n* bit wide data segments while communicating from the serial bus to the parallel bus.

Allowable Subject Matter

12. Claims 6, 8, 9, 21, and 25 are allowed.

13. The following is a statement of reasons for the indication of allowable subject matter.

Referring to claim 6, the prior art does not teach or reasonably suggest in combination with all the limitations that the parallel bus interface is also connected to receive as an input the parallel data segments from the error detector, the parallel bus interface demultiplexing the *n* bit wide parallel data segments from the error detector into *m* bit wide parallel data on the parallel bus.

Response to Arguments

14. The drawings were received on January 24, 2005. These drawings are accepted by the Examiner.

15. Applicant's arguments, with respect to claims 1, 2, 6, 7, 10, 11, 15, and 16 have been fully considered and are persuasive. The rejection under 35 USC 102(b) as being anticipated by Kageyama et al. has been withdrawn.

16. Applicant's arguments, with respect to the rejection(s)of claim(s) 3-5 and 12-14 under 35 USC 102(b) as being anticipated by Göetz et al. have been fully considered

and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection has been made.

17. On page 14, under the section REMARKS, the Applicant argues that neither Göetz et al. nor Carlton et al. teach structure elements and method steps that define an interface between a parallel and serial bus that utilizes a narrow width parallel bus and the multiplexing and demultiplexing associated therewith. The Examiner respectfully disagrees for at least the rejection given above. Further, the interface between a parallel and serial bus that utilizes a narrow width parallel bus and the multiplexing and demultiplexing associated therewith has not been claimed in claims 1 and 10.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

ok to be entered MM 4/14/05

FIG.2